MULTIMEDIA UNIVERSITY

STUDENT ID NO

					1	1	0	9	1

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2018/2019

TSN1101 – COMPUTER ARCHITECTURE AND ORGANIZATION

(All sections / Groups)

1 MARCH 2019
9.00 a.m - 11.00 a.m
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 18 pages with 4 Questions only.

2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please print all your answers in the Answer Booklet provided.

QUESTION 1

a) An address of a memory location is represented in hexadecimal as $(B7F6)_{16}$, Identify the address in Binary, Octal and Decimal representations.

[1.5 marks]

b) Perform the following conversions and complete the table.

Decimal	Excess 3 code	Binary	Gray code
36.375			

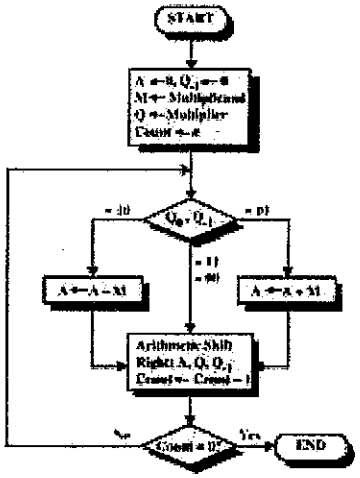
[1.5 marks]

c) Perform the multiplication of two 4-bit twos complement numbers given below. Use Booth's algorithm (Flowchart is given below).

Multiplicand (M) = $(1101)_2$ **(-3 in decimal)**

Multiplier (Q) = $(1011)_2$ **(-5 in decimal)**

Continued ...



[4 marks]

Continued ...

d) Boolean expression for 2-input XOR gate is **F = X'Y + XY'**. Implement **2-input 'XOR gate'** using **only 'NAND' gates** by performing the following:

(i) Identify the **'NAND' form** of the above Boolean expression
(ii) Draw the **logic diagram** using only 'NAND' gates.

[2+2 marks]

e) Assume that a job applicant has to go through three different assessments before obtaining the acceptance result for a job. Assume that applicant has marked 1 for the result of assessment if he/she fulfil that requirement else 0. He/She has to get minimum of two 1's in the assessment results in order to obtain the job. Input signal lines indicate the result of assessments and the output signal line indicate the acceptance result of the job. The output should be 1 if the applicant fulfils the requirement and 0 if he/she rejected.

Continued ...

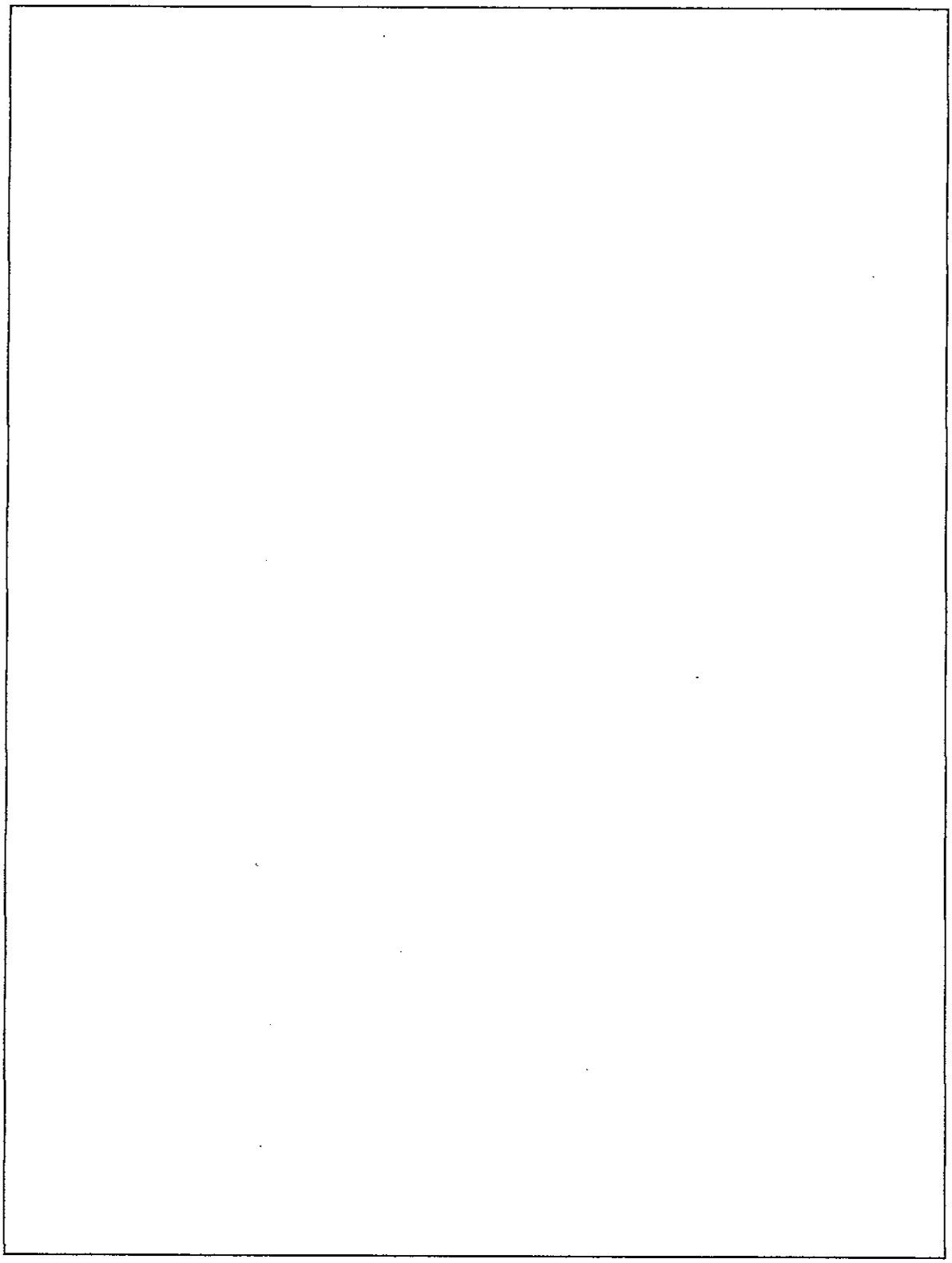
(i) Draw the **truth table** for the above problem indicating all possible combinations for the result of assessments and the corresponding assessments result of the job.

(ii) Minimize the expression into **simplified Sum-of-Products (SOP) form.**

(iii) Construct a logic diagram using **AND-OR gate network.**

[1+2+1 marks]

Continued ...



Continued ...

QUESTION 2

a) Implement the following Sum of Products Boolean expression, using an 8×1 multiplexer.

$$K = \bar{W}\bar{X}YZ + \bar{W}X\bar{Y}Z + \bar{W}XYZ + W\bar{X}Y\bar{Z} + WX\bar{Y}\bar{Z} + WXYZ$$

Perform the following steps for the implementation:

i) Construct the truth table and evaluate the output, K as 0, 1, variable Z or the complement of variable Z.

ii) Draw the connection diagram using an 8×1 multiplexer.

[2+2=4 marks]

Continued ...

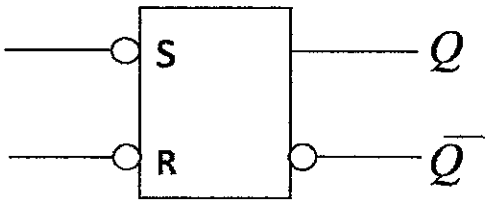
b) Assume that IEEE 754-32 bit single-precision format (as given below) is used for representing floating-point numbers.

Sign	Biased exponent	Mantissa / Significand
1 bit	8 bit2	23 bit2

For the given binary number $(1100\ 0100)_2$
(i) Identify the **normalized form.**
(ii) Identify the **8-bit biased exponent**.

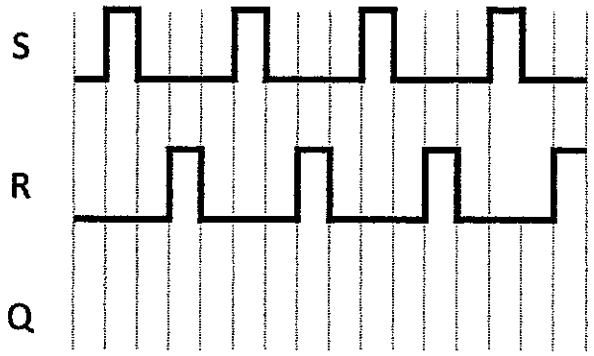
[2 marks]

c) Complete the following timing diagram by applying the waveforms to the below S-R latch. Assume that Q starts with LOW. (Draw the waveforms in the answer booklet)



[2 marks]

Continued ...



Continued ...

d) Design a **3-bit synchronous counter** using **J-K flip-flops** that produce the following sequence: **001,111,100, 010**, and **repeat**. The undesired states must always go to DON'T CARES on the next clock. Your design should include:

(i) **State Transition Diagram** showing all possible states, including those that are not part of the desired counting sequence.

[1 mark]

(ii) Write the **Excitation Table** for J-K flip flop

[1 mark]

(iii) Write **Circuit Excitation Table** for J_A, J_B, J_C, K_A, K_B, K_C by using Present States and Next
States where C is MSB and A is LSB.

[2 marks]

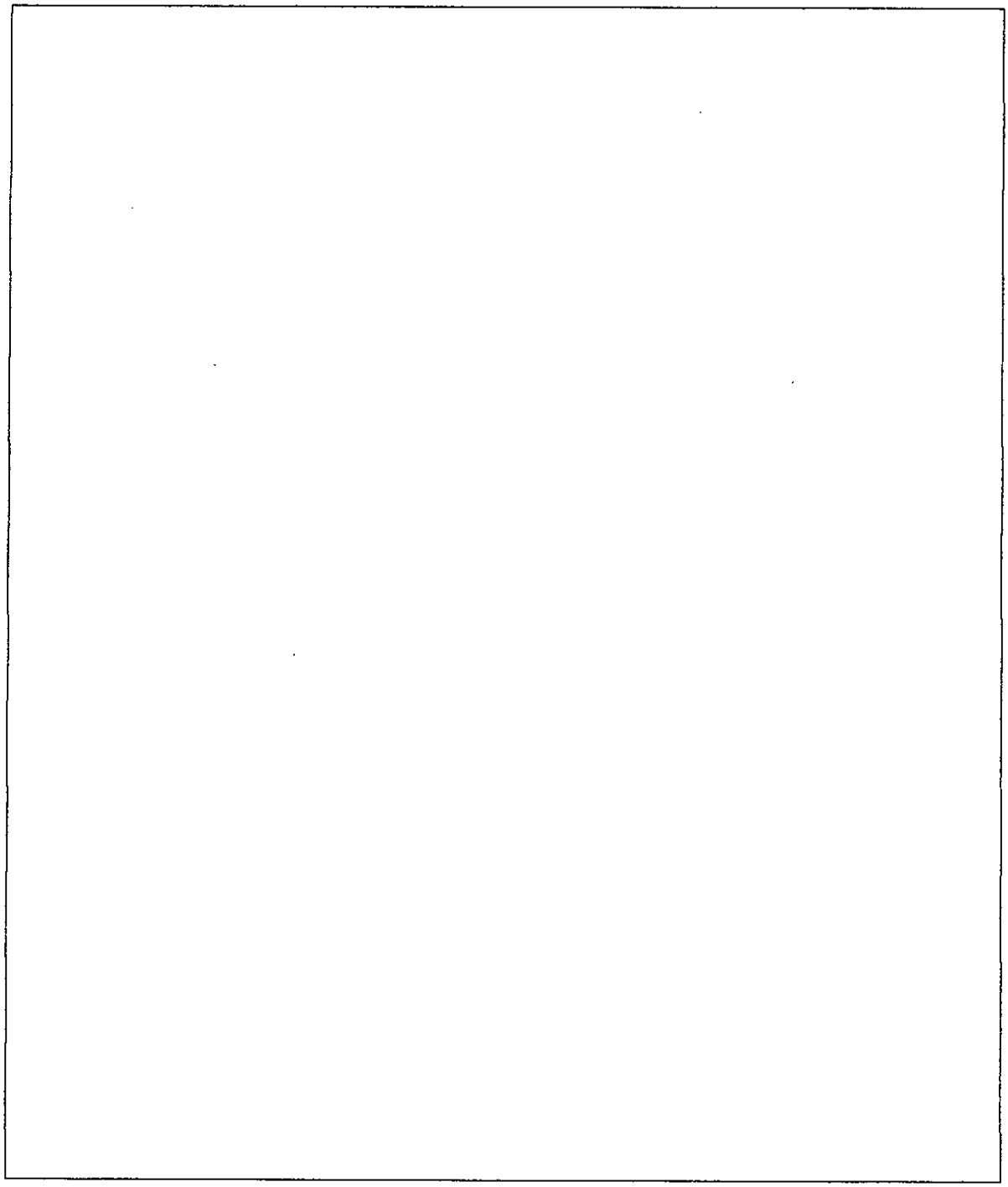
(iv) Perform **Karnaugh Map simplification** for each of J_A, J_B, J_C, K_A, K_B, K_C inputs.

[2 marks]

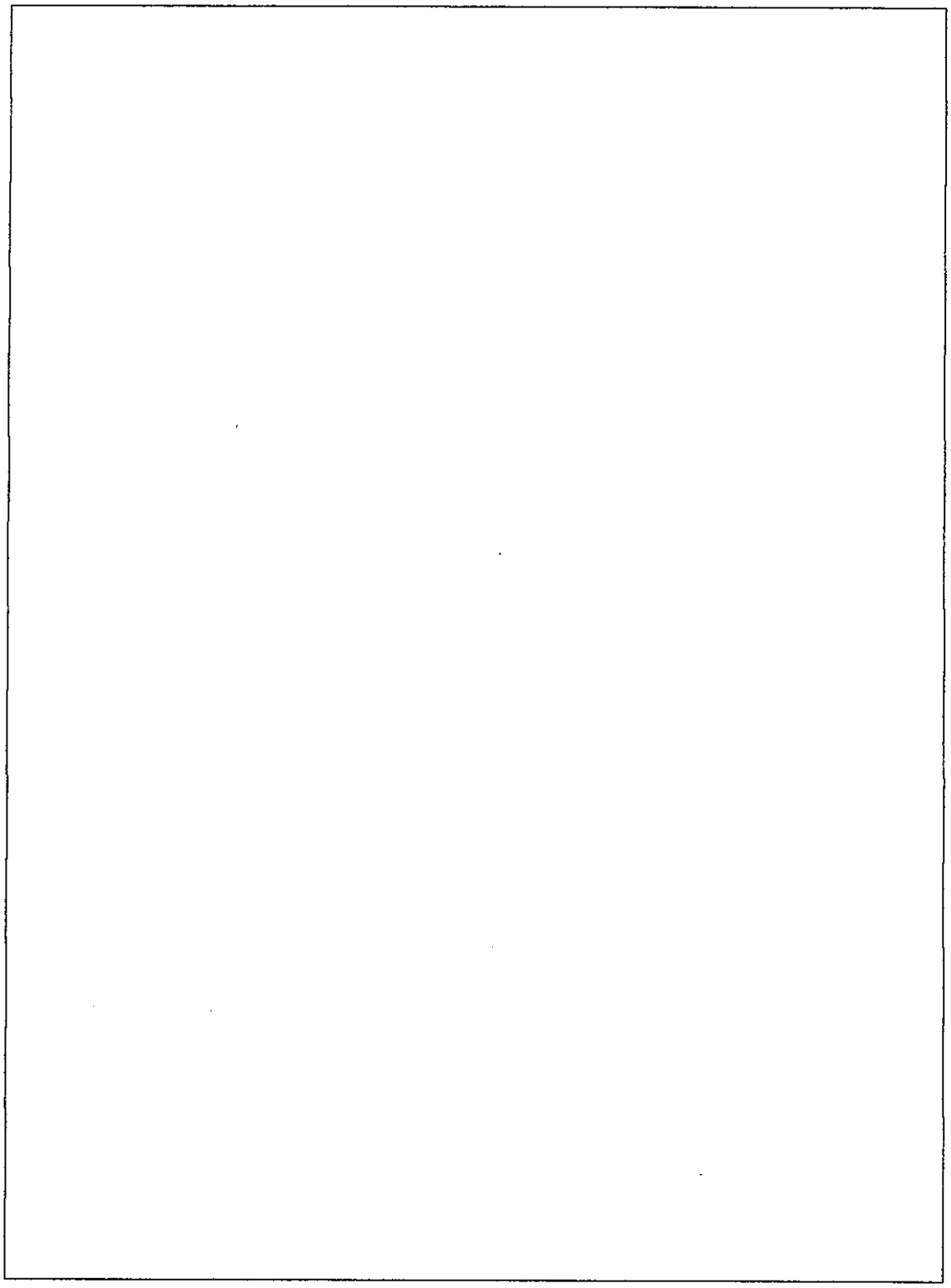
(v) Draw the **Logic Circuit diagram** using J-K flip flop with simplified expressions.

[1 mark]

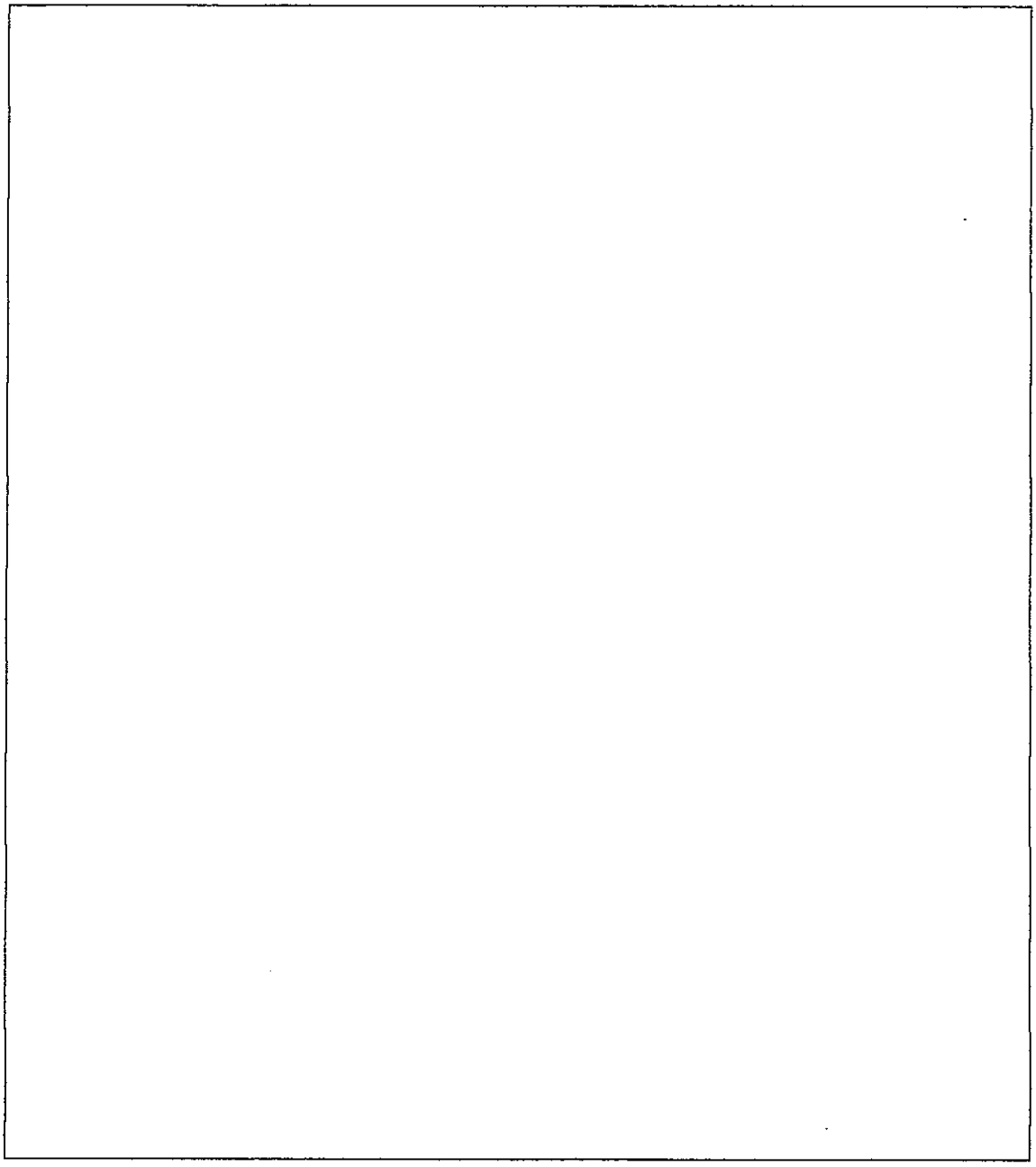
Continued ...



Continued ...



Continued ...



Continued ...

QUESTION 3

a) The processor does the actual work by executing instructions specified in the program. The processing required for a single instruction is called an instruction cycle. Draw and explain a simplified two step instruction cycle.

[3 marks]

b) Assume that a processor that employs a memory address register (MAR), a memory buffer register (MBR), a program counter (PC), and an instruction register (IR). List the sequence of events that happen during the interrupt cycle.

[3 marks]

Continued...

c) Assume a five-stage pipeline (fetch instruction, decode, fetch operand, execute & write). Draw a timing diagram to show how many units are needed for four instructions.

[2 marks]

d) Assume that a processor employs a memory address register (MAR), a memory buffer register (MBR), a program counter (PC), and an instruction register (IR), supporting only one-address instructions. List the symbolic sequence of micro-operations for an interrupt cycle.

[4 marks]

Continued...

e) Assume that Word 55 contains 44, Word 44 contains 33, Word 33 contains 22, and Word 22 contains 55. Given the memory values above and a one-address machine with an Accumulator (Register A), what values do the following instructions load into the Accumulator?

i) LOAD IMMEDIATE 44
ii) LOAD DIRECT 33
iii) LOAD INDIRECT 22
iv) LOAD IMMEDIATE 22
v) LOAD DIRECT 44
vi) LOAD INDIRECT 33

[3 marks]

Continued...

QUESTION 4

a) Given the following registers and a two-address machine, give your program to compute $Z = (W + X)(Y + P \times Q)/(Y - X)$. Available instructions are given below:

   a. Registers: A, B and C
   b. Instructions: MOV R1, DATA; MOV R1, R2; ADD R1, R2; SUB R1,R2; MUL R1,R2 and DIV R1,R2

Store the result in Register A. (Hint: Instruction format – opcode destination, source)
[2.5 marks]

Continued...

b) Devices are connected to the computer through I/O modules. How are devices identified? List and describe the four techniques for device identification.

[4 marks]

c) Write ARM instructions to add the values in memory addresses 0x1000 and 0x2000 respectively and store the result in memory addresses 0x3000.

[4 marks]

Continued...

d) State any **three (3)** categories of instruction set from the aspect of functionality. List any **two (2)** operations from each category.

[3 marks]

e) What is the differences among simple instruction pipelining, superscalar, and simultaneous multithreading.

[1.5 marks]

End of Page.